Claims

What is claimed is:

1. A power amplifier circuit comprising:

an input port for receiving a RF input signal;

an output port for providing a RF output signal therefrom that is an amplified version of the RF input signal;

a control port for receiving a control signal;

a supply voltage input port for receiving a supply voltage;

a temperature sensing circuit for sensing a temperature of the power amplifier circuit and for providing a temperature signal in dependence thereon;

a voltage sensing circuit for sensing a potential of a voltage supply and for providing a sense signal in dependence thereon;

a first amplification stage having a first gain for amplifying one of a signal derived from the RF input signal and the RF input signal to form a first amplified RF signal, the first amplification stage for receiving at least one of the temperature signal and the sense signal and the control signal and for varying the first gain in dependence thereon; and,

a second amplification stage having a second gain for amplifying one of a signal derived from the first amplified RF signal and the first amplified RF signal to form the RF output signal, the second amplification stage for receiving the control signal and other than receiving at least one of the temperature signal and the sense signal for varying the second gain in dependence thereon.

2. A power amplifier circuit according to claim 1, comprising a voltage regulator circuit for receiving the supply voltage and for providing a regulated supply voltage to the first amplification stage.

3. A power amplifier circuit according to claim 1, comprising a voltage regulator circuit for receiving the supply voltage and for providing a regulated supply voltage to the second amplification stage.

4. A power amplifier circuit according to claim 1, comprising a voltage regulator circuit for receiving the supply voltage and for providing a regulated supply voltage to the at least one of the first amplification stage and the second amplification stage.

5. A power amplifier circuit according to claim 2, wherein the regulator circuit comprises a FET having one of the drain and source terminals thereof coupled to the supply voltage input port for receiving the supply voltage and the other of the drain and source terminals thereof coupled to the first amplification stage for providing of the regulated supply voltage thereto.

6. A power amplifier circuit according to claim 5, wherein the regulator circuit comprises an operational amplifier circuit, the operational amplifier circuit having a first input port, a second input port and an output port, the first input port thereof coupled to the control port for receiving the control signal and the output port thereof coupled to a gate terminal of the FET.

7. A power amplifier circuit according to claim 6, comprising a first summing circuit having an output port, a first input port, a second input port and a third input port, the output port thereof coupled to the second input port of the operational amplifier circuit, the first input port thereof coupled to one of the drain and source terminals of the FET for receiving the regulated supply voltage, the second input port thereof coupled to the voltage sensing circuit for receiving the sense signal, and the third input port thereof coupled to the temperature sensing circuit for receiving the temperature signal therefrom.

8. A power amplifier circuit according to claim 6, comprising a feedback sense circuit disposed between one of the drain and source terminals of the FET and the second input port of the operational amplifier circuit, the feedback sense circuit for receiving the regulated supply voltage from the FET.

9. A power amplifier circuit according to claim 8, wherein the feedback sense circuit comprises a voltage divider circuit.

10. A power amplifier circuit according to claim 8, wherein the feedback sense circuit comprises an amplitude shifting circuit.

11. A power amplifier circuit according to claim 8, wherein the feedback sense circuit is integrated on a same die as the power amplifier circuit.

12. A power amplifier circuit according to claim 4, wherein the voltage regulator circuit is integrated on a same die as the power amplifier circuit.

13. A power amplifier circuit according to claim 1, comprising a detector circuit having an input port coupled to the power amplifier circuit output port for determining a RF output signal power level and having an output port for providing an output level signal to at least one of the first amplification stage and the second amplification stage.

14. A power amplifier circuit according to claim 1, comprising a detector circuit having an input port coupled to the power amplifier circuit output port for determining a RF output signal power level and having an output port for providing an output level signal to the first amplification stage.

15. A power amplifier circuit according to claim 1, comprising a detector circuit having an input port coupled to the power amplifier circuit output port for determining a RF output signal power level and having an output port for providing an output level signal to the second amplification stage.

16. A power amplifier circuit according to claim 1, comprising a detector circuit having an input port coupled to the power amplifier circuit output port for determining a RF output signal power level and having an output port for providing an output level signal.

17. A power amplifier circuit according to claim 13, wherein the detector circuit is integrated on a same die as the power amplifier circuit.

18. A power amplifier circuit according to claim 13, wherein the detector circuit comprises at least a difference amplifier circuit having a first input port, a second input port and an output port, the first input port coupled to the detector circuit input port and the second input port for receiving a current mirrored from the RF output signal current.

19. A power amplifier circuit according to claim 18, wherein the detector circuit comprises a second summing circuit having at two input ports and an output port, the at least two input ports thereof coupled to the output ports of the at least a difference amplifier circuit, the output port thereof coupled to at least one of the first amplification stage and the second amplification stage.

20. A power amplifier circuit according to claim 19, wherein the detector circuit comprises:

at least a sense transistor having an emitter terminal, a collector terminal and a base terminal, one of the emitter and collector terminals thereof coupled to ground and the other one of the emitter and collector terminals coupled to the second input port of the at least a difference amplifier circuit;

least a sense resistor disposed in parallel with the first and second input ports of the at least a difference amplifier circuit; and,

a mirror transistor having an emitter terminal, a collector terminal and a base terminal, one of the emitter and collector terminals thereof coupled to ground and the other one of the emitter and collector terminals coupled to the input port of the detector circuit, and the base terminal of the current mirror transistor is coupled to the base terminal of the at least a sense transistor, where the mirror transistor is for current mirroring RF output signal current.

21. A power amplifier circuit according to claim 1, wherein each amplification stage comprises at least a transistor having an emitter terminal, a collector terminal and a base terminal having, one of the emitter and collector terminals coupled to one of the supply voltage and regulated supply voltage and the other one of the emitter and collector terminals coupled to ground.

22. A power amplifier circuit according to claim 21, wherein each amplification stage comprises at least a current source coupled to the base terminal of the at least a transistor.

23. A power amplifier circuit according to claim 22, wherein the at least a current source is integrated on a same die as the power amplifier circuit.

24. A power amplifier circuit according to claim 1, wherein each amplification stage comprises at least a transistor having a drain terminal, a source terminal and a gate terminal, one of the source and drain terminals coupled to one of the supply voltage and regulated supply voltage and the other one of the source and drain terminals coupled to ground.

25. A power amplifier circuit according to claim 24, wherein each amplification stage comprises at least a voltage source coupled to the gate terminal of the at least a transistor.

26. A power amplifier circuit according to claim 25, wherein the at least a voltage source is integrated on a same die as the power amplifier circuit.

27. A power amplifier circuit according to claim 1, comprising a capacitor disposed between the first amplification stage and the second amplification stage.

28. A power amplifier circuit according to claim 1, wherein the voltage sensing circuit and the temperature sensing circuit and the first amplification stage and the second amplification stage are integrated on a same die.

29. A method of operating a multi amplification stage amplifier circuit comprising the steps of:

receiving of a control signal having a control signal magnitude;

providing a first amplification stage having a first gain;

receiving one of a signal derived from a RF input signal and a RF input signal for amplification using the first amplification stage;

amplifying the one of a signal derived from the RF input signal and the RF input signal using the first amplification stage to form a first amplified RF signal, the amplifying of the one of a signal derived from the RF input signal and the RF input signal performed in conjunction with a step of compensating of the first amplification stage for at least two of temperature and supply voltage and control signal magnitude;

providing a second amplification stage having a second gain;

receiving of the first amplified RF signal using the second amplification stage; and,

amplifying one of a signal derived from the first amplified RF signal and the first amplified signal using the second amplification stage to form a RF output signal, the amplifying of the one of a signal derived from the first amplified RF signal and the first amplified signal performed in conjunction with a step of other than compensating of the second amplification stage for at least one of temperature and supply voltage fluctuations.

30. A method according to claim 29, wherein the step of compensating comprises the step of varying the gain thereof.

31. A method according to claim 30, wherein the first amplification stage is compensated for temperature and supply voltage fluctuation and the second amplification stage is compensated for control signal magnitude.

32. A method according to claim 29, comprising the steps of:

receiving of a regulated supply voltage by the first amplification stage; and,

other than receiving of the regulated supply voltage by the second amplification stage.

33. A method according to claim 32, comprising the step of varying of the regulated supply voltage in dependence upon the control signal.

34. A method according to claim 29, comprising the step of varying of the first gain in dependence upon the control signal.

35. A method according to claim 29, comprising the step of varying of the second gain in dependence upon the control signal.

36. A method according to claim 29, wherein the step of compensating comprises the steps of:

sensing a temperature of the power amplifier circuit to provide a temperature signal; and,

varying the first gain in dependence upon the temperature signal.

37. A method according to claim 29, wherein the step of receiving of a regulated supply voltage comprises the steps of:

sensing a temperature of the power amplifier circuit to provide a temperature signal; and,

varying the regulated supply voltage in dependence upon the temperature signal.

38. A method according to claim 32, wherein the step of receiving of the regulated supply voltage comprises the steps of:

sensing a supply voltage potential to provide a sense signal; and,

varying the regulated supply voltage in dependence upon the sense signal.

39. A method according to claim 29, comprising the steps of:

sensing a supply voltage potential to provide a sense signal; and,

varying the first gain of the first amplification stage in dependence upon the sense signal.

40. A method according to claim 32, comprising the steps of:

sensing a temperature of the power amplifier circuit to provide a temperature signal;

sensing a potential of the supply voltage to provide a sense signal;

receiving the regulated supply voltage;

summing the received portion of the regulated supply voltage and the sense signal and the temperature signal to form a summed signal; and,

varying the regulated supply voltage in dependence upon the summed signal.

41. A method according to claim 29, comprising the steps of:

detecting the RF output signal power level to provide an output level signal; and,

providing the output level signal to the first amplification stage.

42. A method according to claim 41, comprising the step of varying the first gain of the first amplification stage in dependence upon the output level signal.

43. A method according to claim 41, wherein the step of detecting comprises the steps of:

current mirroring the RF output signal current to form a RF output signal mirror current; and,

logarithmically amplifying the RF output signal mirror current to provide the output level signal to the first amplification stage.

44. A method according to claim 29, comprising the steps of:

detecting the RF output signal power level to provide an output level signal; and

providing the output level signal to the second amplification stage.

45. A method according to claim 44, comprising the step of varying the second gain of the second amplification stage in dependence upon the output level signal.

46. A method according to claim 44, wherein the step of detecting comprises the steps of:

current mirroring the RF output signal current to form a RF output signal mirror current; and,

logarithmically amplifying the RF output signal mirror current to provide the output level signal to the second amplification stage.

47. A method according to claim 44, wherein the step of detecting comprises the steps of:

detecting a first RF output signal power level to provide a first output level signal;

detecting a second RF output signal power level to provide a second output level signal;

summing the detected first output level signal and the detected second output level signal to form a summed signal; and,

providing the output level signal in dependence upon the summed signal.

48. A method according to claim 44, wherein the step of detecting comprises the steps of:

providing a first resistor having a first resistance;

detecting a first mirror current from the RF output current using the first resistance of the first resistor;

providing a second resistor having a second resistance;

detecting of a second mirror current from the RF output using the second resistance of the second resistor;

summing the detected first mirror current and the detected second mirror current to provide a summed signal; and,

forming the output level signal in dependence upon the summed signal.

49. A method according to claim 29, comprising the step of varying the first gain and the second gain to other than vary output power of the RF output signal.